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BURIED CHANNEL DEVICES AND A PROCESS FOR THEIR FABRICATION SIMULTANEOUSLY WITH SURFACE CHANNEL DEVICES TO PRODUCE TRANSISTORS AND CAPACITORS WITH MULTIPLE ELECTRICAL GATE OXIDES

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BURIED CHANNEL DEVICES AND A PROCESS FOR THEIR FABRICATION SIMULTANEOUSLY WITH SURFACE CHANNEL DEVICES TO PRODUCE TRANSISTORS AND CAPACITORS WITH MULTIPLE ELECTRICAL GATE OXIDES

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FIELD OF THE INVENTION

The present invention relates generally to integrated circuits (ICs) and the methods for fabricating them on semiconductor substrates. More specifically, the present invention relates to devices having a buried channel fabricated on a semiconductor substrate and methods for fabricating them.

BACKGROUND OF THE INVENTION

Integrated circuits (ICs) are ubiquitous in products ranging from personal computers to portable digital assistants ("PDAs") to cellular telephones. As the functional boundaries between different products have gradually blurred, with portable telephones now providing internet access and PDAs also functioning as global positioning system receivers, the complexity of the ICs in these products has increased at a nearly exponential rate. Often, a single IC must operate at high speed, use little power, have a high level of circuit density and, in many cases, also have both analog and digital functions incorporated into it.

As the number of functions performed by these "systems-on-a-chip" has increased, the number of different devices that must be fabricated on the same semiconductor substrate has also increased, such devices including multiple types of transistors and low leakage capacitors. Each different device that must be fabricated on the same IC complicates the already complicated semiconductor processing flow. One particular problem of fabricating so many different devices on the same IC at the same time is that the different devices need gate oxides of different thickness.

Although the formation of oxides, particularly silicon dioxide, in silicon semiconductor processing is well known and technically straightforward, fabricating oxides of different thickness on the same semiconductor wafer during processing is difficult. One known method for fashioning oxides of different thickness is known as "grow-etch-grow." In this method, a first gate oxide layer is grown on a semiconductor wafer. The wafer is then masked in a known manner and the first layer gate oxide is etched away from certain areas. The mask is then stripped and a second, additional oxide layer is grown on the wafer. The cycle is repeated until the different oxide layers have reached their desired thickness.

For the particular device known as a 1-T random access memory ("RAM"), wherein a capacitor stores an individual bit of data, the capacitors are fabricated using a poly-insulator-poly ("PIP") process. The PIP method fabricates capacitors by etching an additional trench within the shallow trench isolation ("STI") region of the wafer. A first polysilicon layer is deposited in the additional trench. A dielectric layer is then formed, followed by as many additional trenches, polysilicon and dielectric layers as necessary. This succession of layers forms the desired capacitor.

Both methods have significant drawbacks. Each oxide growth cycle is charged against the process temperature budget, as oxide growth requires relatively high temperatures that affect concentrations of implanted dopants in other regions of the wafer. Every additional process step increases fabrication costs both directly and indirectly, as manufacturing yield declines with each additional manufacturing step.

Particularly as semiconductor processing technology moves to sub-180 nanometer (nm) technologies, there is a need to create devices on the same wafer with different effective oxide thickness without increasing the number of process steps overall.

SUMMARY OF THE INVENTION

In a first embodiment of the present invention, buried channel NMOS devices are fabricated. These buried channel NMOS devices are fabricated with a p-type substrate, an n-type implant in the top portion (approximately 400 to 1000 Å deep) of the substrate, and an insulating gate dielectric above the n-type implant. An n-type or p-type doped polysilicon gate electrode is formed on top of the insulating gate dielectric. The n-type implant region is doped in such a way that it is depleted of charge carriers when the device's gate electrode is at the same potential as the well (zero bias). When the gate electrode is biased $+V_e$ with respect to the device's well, a conducting channel of mobile electrons is formed in a portion of the buried layer. This type of biasing is known as inversion bias as the charge carriers are of the opposite type than the p-well. Under inversion bias, the buried channel silicon region is partially depleted of charge carriers, which effectively adds to the thickness of the gate dielectric layer. A capacitor or transistor fabricated according to this buried channel teaching behaves in a manner electrically equivalent to a capacitor or transistor fabricated with a thicker dielectric.

By using both conventional devices and devices incorporating the buried channel of the present invention on the same IC, effective additional dielectric thickness is obtained without the need to physically grow a thicker dielectric. The thicker dielectric created by the buried channel also reduces the amount of current leakage between the gate electrode and the substrate in capacitors, which is a significant problem when dielectric thickness is less than or equal to about 22 Å. The reduced leakage makes buried channel capacitors very useful for such applications as filter capacitors in phase locked loops ("PLLs"), storage capacitors for 1-transistor RAM (1-T RAM) and voltage stabilizing on-chip capacitors.

PMOS transistors and capacitors can be constructed according to the present invention in a manner similar to that described for NMOS transistors and capacitors by substituting n-type doping for p-type and visa versa. This leads to the fabrication of CMOS devices with multiple effective dielectric thicknesses on the same substrate.

By greatly reducing the number of extra oxidation steps necessary to create a dielectric layer of desired thickness, the present invention reduces process cost, increases process yield

and reduces process temperature, which is a great advantage with respect to sub-180 nm technologies brief description of the drawings

BRIEF DESCRIPTION OF THE DRAWINGS

The invention, together with further advantages thereof, may best be understood by reference to the following description taken in conjunction with the accompanying drawings in which:

Fig. 1 is a cross-sectional drawing of a semiconductor wafer at the beginning of processing, according to a first embodiment of the present invention;

Fig. 2 is a cross-sectional drawing of the semiconductor wafer shown in Fig. 1, undergoing a further step in its processing;

Fig. 3 is a cross-sectional drawing of the semiconductor wafer shown in Fig. 2, undergoing a further step in its processing;

Fig. 4 is a cross-sectional drawing of the semiconductor wafer shown in Fig. 3, undergoing a further step in its processing;

Fig. 5 is a cross-sectional drawing of the semiconductor wafer shown in Fig. 4, undergoing a further step in its processing;

Fig. 6 is a cross-sectional drawing of the semiconductor wafer shown in Fig. 5, undergoing a further step in its processing;

Fig. 7 is a cross-sectional drawing of the semiconductor wafer shown in Fig. 6, undergoing a further step in its processing;

Fig. 8 is a cross-sectional drawing of the semiconductor wafer shown in Fig. 7, undergoing a further step in its processing;

Figs. 9a and 9b are, respectively, a cross-sectional drawing of the semiconductor wafer shown in Fig. 8 undergoing a further step in its processing and a detail of one device created by the previously illustrated processing steps;

Figs. 10a and 10b are, respectively, a cross-sectional drawing of the semiconductor wafer shown in Fig. 9a undergoing a further step in its processing and a detail of one device created by the previously illustrated processing steps;

Figs. 11a and 11b are cross-sectional drawings of, respectively, a known NMOS transistor and a known MOS capacitor and an NMOS transistor and MOS capacitor fabricated according to an embodiment of the present invention; and

Figs. 12a, 12b, and 12c are, respectively, electron band diagrams of a known surface channel device, a first buried channel device and a second buried channel device.

Use of the same reference number in different figures indicates similar or like elements.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to some presently preferred embodiments of the invention. Examples of preferred embodiments are illustrated in the accompanying drawings. While the invention will be described in conjunction with these preferred embodiments, it will be understood that it is not intended to limit the invention to any particular preferred embodiment. On the contrary, it is intended to cover alternatives, modifications and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. The present invention may be practiced without some or all of these specific details. In other instances, well known process operations have not been described in detail in order not to unnecessarily obscure the present invention.

Fabrication of both N- and P-type buried channel and surface channel devices can be accomplished almost simultaneously. Fig. 1 shows a cross-section of a semiconductor wafer at the beginning of the process used to fabricate devices according to an embodiment of the present invention. P-type substrate 110 has undergone an initial process step to create a plurality of shallow trench isolation (STI) regions 112 in substrate 110. STIs 112 serve to isolate completed devices electrically. A photo-resist is applied to the substrate and then a mask step follows. After removal of the photo-resist from unmasked areas of substrate 110, an N-type well is created by implanting, in this embodiment, phosphorus at an energy level in the range of 200 - 300 KeV and a doping dose of 5 to 10 $*10^{12}/cm^2$. Arrows 114 indicate the location of the N-type well implant.

After the N-type well implant, the remaining photo-resist is removed and the wafer again covered with a photo-resist, which is then masked and selectively removed. As shown in Fig. 2, N-type well 210 is now defined within substrate 110. NMOS buried channel devices 121 and PMOS surface channel devices 122 now receive an n-type implant 115. In this embodiment the n-type implant comprises arsenic at an energy level in the range of 100 to 150 KeV and a dose of 1 to 5 $*10^{12}/cm^2$. This n-type implant 115 for NMOS devices is opposite

to the p-type substrate of these devices. It is this implant 115 that ultimately comprises the buried channel in the finished devices.

After again stripping off the residual photo-resist, reapplying photo-resist and again masking the wafer, wafer 100 appears as shown in Fig. 3. A p-type well is now created in p-type substrate 110 for all NMOS devices, including both surface channel devices 120 and buried channel devices 121. In this embodiment, the p-type well is created using boron at an energy level of 80 to 120 KeV and a dose level of 4 to $8*10^{12}/cm^2$. P-type well 310 is illustrated in Fig. 4.

As is also shown in Fig. 4, residual photo-resist has again been removed, followed by a new coat of photo-resist and another masking operation. PMOS buried channel devices 123 and NMOS surface channel devices 120 now receive a p-type implant 215. This p-type implant uses boron at an energy level of 10 to 25 KeV and a dose level of 1 to $5*10^{12}/cm^2$. This p-type implant 215 for PMOS devices is opposite to its n-type well 210, thereby forming the buried channel portion of the finished device.

Continuing the processing of wafer, residual photo-resist is removed from the wafer. As shown in Fig. 5, a gate oxide is grown and a polysilicon layer 140 is deposited on wafer 100. A photo-resist is then deposited on top of polysilicon layer 140 and masked. An n-type impurity is now implanted into NMOS surface channel devices 120 and NMOS "regular gate" buried channel devices 121, as well as into PMOS "swapped gate" buried channel devices 123. A "regular gate" device is one in which the gate doping is of the opposite type than the well, e.g. an N-type doped gate on a p-type well substrate. A "swapped gate" device is one which has the same type of polysilicon gate implant impurity as that of the device's well. In this embodiment, the n-type impurity is phosphorus, implanted with an energy of 25 to 40 KeV and a dose of 3 to $6*10^{15}/cm^2$.

As shown in Fig. 6, those areas of the wafer that did not receive the n-type implant as shown in Fig. 5 will receive, after the residual photo-resist is stripped off, another coat of photo-resist applied and the new photo-resist masked as necessary, a p-type impurity implant into p-type polysilicon NMOS buried channel device 121, PMOS surface channel devices 122 and p-type polysilicon PMOS buried channel devices 123. In this embodiment, the p-type implant comprises BF_2 at an energy level of 20 to 35 KeV and a dose of 1 to $3*10^{15}/cm^2$.

After the implants shown in Figs. 5 and 6, residual photo-resist is again removed from the wafer, another coat of photo-resist applied and another mask operation performed on the photo-resist layer. After this masking operation, an etching operation removes most of polysilicon layer 140, except n-type gates 150 and p-type gates 250, as shown in Fig. 7. After this selective removal of the polysilicon layer, residual photo-resist is removed and a new layer of photo-resist deposited masked and then selectively removed. Again as shown in Fig. 7, through those areas exposed after the removal of the photo-resist, an n-type lightly doped drain (NLDD) implant goes to the active areas of all NMOS devices 120 and 121, as well as the polysilicon gates 150 of n-polysilicon NMOS surface channel device 120 and n-polysilicon NMOS buried channel device 121. This NLDD implant uses, in this embodiment, arsenic at an energy level of 3 to 7 KeV and a dose of 0.5 to $1.5*10^{15}/cm^2$.

In a very similar fashion, a p-type lightly doped drain (PLDD) implant goes to the active areas of all PMOS devices 122 and 123, as well as to the polysilicon gates 250 of p-polysilicon PMOS surface channel devices 122 and p-polysilicon PMOS buried channel devices 123. This implant step is shown in Fig. 8. This PLDD implant uses BF_2 at an energy level of 3 to 7 KeV and a dose of 1 to $4*10^{14}/cm^2$. The same series of steps of stripping residual photo-resist, applying a new coat of photo-resist and then masking and developing the exposed photo-resist occur before the PLDD implant as they did before the NLDD implant.

Following the NLDD and PLDD implants shown respectively in Figs. 7 and 8 dielectric spacers are defined on the sides of the polysilicon gates as shown in fig. 9a. . Then n-type dopant will be implanted into the source and drain areas 152 of NMOS devices 120 and 121, as well as the polysilicon gates 150 of n-type polysilicon NMOS surface channel devices 120 and n-type polysilicon NMOS "regular gate" buried channel devices 121. A photoresist coat, masking and developing step was applied to the wafer prior to this implant. The process step is shown in Fig. 9a. The n-type dopant in this embodiment is arsenic at an energy level of 40 to 70 KeV and a dose of 2 to $4*10^{15}/cm^2$. A cross section of a completed n-type polysilicon NMOS surface channel device is shown in Fig. 9b, wherein source/drain areas 152 have an N+ dopant concentration and a surface channel lies directly below gate 150.

As shown in Fig. 10a, a similar dopant implant operation is required for the PMOS surface channel devices 122 and buried channel devices 123. After removing the residual photo-resist, another photo-resist layer is applied, masked and developed. A p-type dopant is implanted in the source and drain areas 154 of PMOS surface channel devices 122 and PMOS

buried channel devices 123 as well as in the polysilicon gates 250 of PMOS surface channel devices 122 and "regular gate" buried channel devices 123. This same implant goes to polysilicon gate 250 of "swapped gate" buried channel NMOS devices 121. In this embodiment, the p-type dopant comprises BF_2 at an energy level of 20 to 35 KeV and a dose of 2 to $4*10^{15}/cm^2$. A cross section of a completed P-polysilicon PMOS surface channel device is shown in Fig. 10b, wherein source/drain areas 154 have an p+ dopant concentration and a surface channel lies directly below gate 250. In another embodiment of the "swapped gate", the buried channel NMOS device receives only this p-type implant with no need for the P-Poly implant shown in figure 6.

Fig. 11a shows a cross-section of a known surface channel NMOS transistor 5 and a known MOS capacitor 50. In transistor 5, a p-type substrate 10 is implanted with p-type dopants to form region 20, which region adjusts transistor 5's operating threshold. An insulating gate dielectric 30 is formed above region 20 and a n-type doped polysilicon gate electrode 40 is formed on top of dielectric 30. Source and drain regions 25 complete transistor 5. MOS capacitor 50 is constructed in an identical fashion, with the exception of source and drain regions 25 and doped polysilicon gate electrode 40. In another embodiment of the present invention, the fabrication process would result in the MOS capacitors having source and drain regions around them. In this embodiment, the source and drains would be electrically tied to the capacitor's well.

A cross-section of a buried channel NMOS transistor 70 and buried channel MOS capacitor 80, constructed according to an embodiment of the present invention, is shown in Fig. 11b. To form transistor 70, an n-type implant 74 of from 400 to 1000 Å in depth is formed in p-type substrate 72. Insulating gate dielectric 76 is formed over implant 74 and an n-type or p-type doped polysilicon gate electrode 78 is formed over gate dielectric 76. Drain and source 73 are formed on substrate 72 and complete transistor 70. MOS capacitor is formed in an identical manner to transistor 70, with the exception of source and drain 73 and gate electrode 78.

The n-type implant 74 is doped in such a way that it becomes depleted of charge carriers when gate electrode 78 is biased +Ve with respect to the substrate. This is also known as inversion bias. This silicon region, which is depleted of charge carries, thus adds to the gate dielectric thickness, effectively creating a thicker gate dielectric. Figs. 12a, 12b and 12c present band diagrams from representative devices. Fig. 12a is a band diagram of a known

surface channel device having an n-type gate, a +p-type channel and a +p-type substrate. Under inversion bias there is an increase in free electrons in the channel, resulting in the formation of a conducting channel. Fig. 12b is a band diagram of a buried channel device according to an embodiment of the present invention. The device has a p-type gate, an n-type channel and a p-type substrate. Under the same inversion bias that the known surface channel device shown in Fig. 12a was subjected to, the channel is depleted of charge carriers, effectively making the n-type channel region insulting and adding to the gate insulator thickness. Fig. 12c is a band diagram of a buried channel device constructed according to the present invention and differing from the device characterized in Fig. 12b only in that it has an n-type gate. Consequently, the bias is – Ve, not + Ve. The operation of the device and the effect of the channel in increasing the effective oxide thickness under the chosen operating conditions are identical.

By using conventional and buried channel devices on the same semiconductor die, additional dielectric thickness can be obtained without the necessity of physically growing an additional layer of dielectric material. The effectively thicker dielectric provided by the buried channel also reduces the amount of current leakage between the gate electrode and the substrate. Such leakage is a major problem when dielectric oxides thinner than or equal to about 22 Å are used. This reduced leakage current makes capacitors constructed with buried channels according to the present invention attractive for applications such as filter capacitors in phase locked loops (PLLs), storage capacitors for 1-transistor random access memories (RAM) and voltage stabilizing on-chip capacitors.

As shown in Figs. 1 through 10b, PMOS and NMOS transistors and capacitors can readily be fabricated on the same semiconductor wafer without significantly increasing process complexity. These buried channel devices are constructed without adding any steps to the CMOS process flow. Buried channel NMOS devices use the same channel implant as the surface channel PMOS devices, namely an n-type dopant such as As or P. Thus, only the masks used in fabrication require modification. This is accomplished by opening an appropriate window in the mask artwork used for the channel implant. The buried channel PMOS devices use the same channel implant as the surface channel NMOS devices, primarily a p-type dopant such as boron. If the buried channel NMOS device needs to be constructed with a p-type gate doping, the p-type dopant of the surface channel PMOS gate device can be used by opening a window in the mask artwork used for this doping step. In a similar fashion,

n-type gate doping for a buried channel PMOS device can be done with the n-type doping of surface channel NMOS devices. Using an embodiment of the present invention with standard CMOS process flow, NMOS and PMOS surface channel devices, NMOS buried channel devices with n-type gate doping, NMOS buried channel devices with p-type gate doping, PMOS buried channel devices with p-type gate doping and PMOS buried channel devices with n-type gate doping have been fabricated, with the buried channel devices exhibiting an effectively higher gate dielectric thickness. Given that only relatively minor modifications are needed to incorporate the buried channel taught herein into known CMOS process flows, it will also be a straightforward process to incorporate the present invention's buried channel technology into existing IC fabrications processes and existing ICs. Such modification may improve performance and decrease manufacturing cost.

Although the present invention has been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. Therefore, the described embodiments should be taken as illustrative and not restrictive, and the invention should not be limited to the details given herein but should be defined by the following claims and their full scope of equivalents.